Notice of Allowability	Application No.	Applicant(s)	
	09/847,487	KOH ET AL.	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *October 24, 2005*.

2. ☒ The allowed claim(s) is/are *1,3,7,11,12,14,15,18,22,24,25 and 27*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☒ Other *Clean copy of allowed claims*.

DETAILED ACTION

Introduction

1. This communication is in response to the Applicants' communication dated October 24, 2005 giving a notice of appeal and requesting a pre-appeal brief review. Claims 1-27 of the application are pending.

Examiner's Amendment

2. Authorization for this examiner's amendment was given in a telephone conversation by Mr. James Clingan on December 6, 2005.

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to the applicants, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

3 In the claims:

Replace Claim 1 with:

1. A method for testing an integrated circuit, comprising:

providing a stimulus to a test bench;

providing a device model corresponding to the integrated circuit to the test bench;

in response to applying the stimulus to the device model through the test bench, generating captured simulation, the captured simulation comprising strobe timing information, opcode information, mixed signal information, and internal memory content information;

automatically generating tester software corresponding to the integrated circuit using the captured simulation;

generating a virtual test software;

testing the device model of the integrated circuit and debugging and verifying the tester software using the virtual test software; and

testing the integrated circuit using the tester software.

Claim 2: (Cancelled).

Claims 4-6: (Cancelled).

Claims 8-10: (Cancelled).

Replace Claim 12 with:

12. A method for testing an integrated circuit, comprising:

generating a captured simulation in response to applying a stimulus to a device model of the integrated circuit, wherein the captured simulation comprises strobe timing information, opcode information, mixed signal information, and internal memory content information, the captured simulation generated in response to stimulus applied to the device model through a test bench;

generating data patterns based on strobe timing information, opcode information, mixed signal information, and internal memory content information, the data patterns capable of being retargettable for a plurality of post-processing tools;

generating a first formatted pattern file based on the data patterns;

automatically generating tester software corresponding to the integrated circuit using the first formatted pattern file;

testing the device model of the integrated circuit and debugging and verifying the tester software using virtual test software; and

testing the integrated circuit using the tester software in an automatic test equipment (ATE) tester.

Claim 13: (Cancelled).

Claims 16-17: (Cancelled).

Replace Claim 18 with:

18. A testing system for testing an integrated circuit, comprising:

simulation means for generating a captured simulation in response to applying a stimulus to a device model of the integrated circuit;

first instruction means for receiving the captured simulation wherein the captured simulation comprises strobe timing information, opcode information, mixed signal information, and internal memory content information, the captured simulation generated in response to stimulus applied to a device model through a test bench;

second instruction means for generating data patterns based on strobe timing information, opcode information, mixed signal information, and internal memory content information, the data patterns capable of being retargettable for a plurality of post-processing tools;

third instruction means for generating a first formatted pattern file based on the data patterns;

fourth instruction means for automatically generating tester software corresponding to the integrated circuit using the first formatted pattern file;

fifth instruction means for testing the device model of the integrated circuit and debugging and verifying the tester software using a virtual test software; and

an automatic test equipment (ATE) tester for testing the integrated circuit using the tester software.

Claims 19-21: (Cancelled).

Replace Claim 22 with:

22. A testing system for testing an integrated circuit, comprising:

first instruction means for receiving a stimulus;

second instruction means for receiving a device model corresponding to an integrated circuit;

third instruction means for generating simulation parameters in response to applying the stimulus to the device model;

fourth instruction means for creating captured simulation based on the simulation parameters, the captured simulation comprising strobe timing information, opcode information, mixed signal information, and internal memory content information; and

fifth instruction means for automatically generating tester software corresponding to the integrated circuit using the captured simulation;

sixth instruction means for testing the device model of the integrated circuit and debugging and verifying the tester software using a virtual test software; and

an automated tester means for testing the integrated circuit using the tester software.

Claim 23: (Cancelled).

Replace Claims 24 and 25 with:

24. The testing system of claim 22, wherein the captured simulation captures all communication between the stimulus and the device model through a standard reusable test bench.

25. The testing system of claim 24, wherein all communication with the device model occurs through the standard reusable test bench.

Claim 26: (Cancelled).

A clean copy of the allowed claims is attached.

Reasons for Allowance

4. Claims 1, 3, 7, 11-12, 14-15, 18, 22, 24-25 and 27 of the application are allowed over prior art of record.

5. The following is an Examiner's statement of reasons for the indication of allowable subject matter:

The closest prior art of record shows:

(1) a verifier of test patterns used for testing an integrated circuit and a test pattern verifying method for rapidly verifying test patterns prepared for a semiconductor tester using the logic simulation data generated during the design stage by CAD technique, without using an actual semiconductor tester; the device logic simulator has a test bench through which test vectors are applied to the device to test the design of the device and produce the device response; after the device is manufactured, it is tested on a LSI tester which applies a test pattern to the device and compares the resulting output to an expected value; preparing a program to generate the test pattern and a pattern of expected values could be omitted if the data generated during the logic simulation is used for testing the devices on the LSI tester; the test pattern in the LSI tester and the pattern of expected results could be obtained from the dump file generated during logic simulation; the data generated in logic simulation are on the event basis in the form of waveforms of test patterns applied to the individual pins and outputs from the device model at times when events occur; the LSI tester uses test patterns on the cycle basis in which the data is

applied for each test cycles using logic values of test patterns applied to the pins ; therefore, the test patterns and expected values generated in the logic simulation are converted from the event basis to the cycle basis; then the data generated for the LSI tester are verified using an LSI tester simulator which is a software tool (**Araki et al.,** U.S. Patent Application 2001/0007972);

(2) an IC tester organizing an IC test into a succession of test cycles, each test cycle being subdivided into four segments; the tester has a separate tester channel for carrying out a test activity at each pin of the IC during each segment of the test cycle; the tester also includes a separate pattern generator for each channel for generating a set of four vectors at the start of each cycle; each of the four vectors tell the channel the activity it is to carry out during a separate one of the four test cycle segments; the test vectors are stored in a vector memory; four opcodes instruction pattern generator supplies to each vector pattern generator for each test cycle the vectors that are to be applied to the corresponding tester channel at the start of the test cycle (**Gruodis et al.,** U.S. Patent 6,092,225); and

(3) a multipurpose configurable bus simulation bus functional model for testing a circuit; the bus function model uses a configurable data structure to interact with the device being tested by providing a high level test generation routine defined by the bus interface specified; the configurable data structure allows for verification of both signal timing and functional operation of bus specifications; the data structure utilizes a parameterized and standardized method that allows the variations and multiple instances of test bench models to be generated and instantiated in a design test environment (**Reise et al.,** U.S. Patent 6,678,625).

Additional state of the art reviewed and considered by the Examiner is found in U.S. Patent Application 2002/0112209; U.S. Patent Application 2001/0010080; U.S. Patent 6,876,214; U.S. Patent 6,868,513; U.S. Patent 6,708,305; U.S. Patent 6,629,277; U.S. Patent 6,622,271; U.S. Patent 6,438,048; U.S. Patent 6,370,675; U.S. Patent 6,256,760; U.S. Patent Application 2003/0177426; U.S. Patent Application 2003/0066003; U.S. Patent Application 2002/0073374.

None of these references taken either alone or in combination with the prior art of record discloses a method for testing an integrated circuit, specifically including:

"in response to applying the stimulus to the device model through the test bench, generating captured simulation, the captured simulation comprising strobe timing information, opcode information, mixed signal information, and internal memory content information;

automatically generating tester software corresponding to the integrated circuit using the captured simulation".

None of these references taken either alone or in combination with the prior art of record discloses a method for testing an integrated circuit, specifically including:

"generating a captured simulation in response to applying a stimulus to a device model of the integrated circuit, wherein the captured simulation comprises strobe timing information, opcode information, mixed signal information, and internal memory content information, the captured simulation generated in response to stimulus applied to the device model through a test bench;

generating data patterns based on strobe timing information, opcode information, mixed signal information, and internal memory content information, the data patterns capable of being retargettable for a plurality of post-processing tools;

generating a first formatted pattern file based on the data patterns;

automatically generating tester software corresponding to the integrated circuit using the first formatted pattern file".

None of these references taken either alone or in combination with the prior art of record discloses a testing system for testing an integrated circuit, specifically including:

"first instruction means for receiving the captured simulation wherein the captured simulation comprises strobe timing information, opcode information, mixed signal information, and internal memory content information, the captured simulation generated in response to stimulus applied to a device model through a test bench;

second instruction means for generating data patterns based on strobe timing information, opcode information, mixed signal information, and internal memory content information, the data patterns capable of being retargettable for a plurality of post-processing tools;

third instruction means for generating a first formatted pattern file based on the data patterns;

fourth instruction means for automatically generating tester software corresponding to the integrated circuit using the first formatted pattern file".

None of these references taken either alone or in combination with the prior art of record discloses a testing system for testing an integrated circuit, specifically including:

"fourth instruction means for creating captured simulation based on the simulation parameters, the captured simulation comprising strobe timing information, opcode information, mixed signal information, and internal memory content information; and

fifth instruction means for automatically generating tester software corresponding to the integrated circuit using the captured simulation".

6. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard, can be reached on 571-272-3749. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to TC 2100 Group receptionist: 571-272-2100.

K. Thangavelu
Art Unit 2123
December 6, 2005

Paul L. Rodriguez 12/12/05
Primary Examiner
Art Unit 2125